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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,684	08/19/2003	Robert A. Dunstan	110349-133959	6456

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

MAIL DATE	DELIVERY MODE
04/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,684	DUNSTAN ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL REJECTION

1. Claims 1-15 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. Claims 1-6, 9 and 10-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Bui (Bui), U.S. patent no. 6,763,478[1].

As per claim 1, Bui teaches a method of operation comprising:

powering a hardware element of a device with a power supply of the device [figures 1, 2; col. 1, lines 25-30, 56-58];

operating the hardware element at a first power consumption level while AC is present at the power supply [col. 1, lines 56-67];

monitoring for absence of AC to the power supply [col. 4, lines 26-29];

generating a signal to indicate AC failure on detection of absence of AC to the power supply [col. 3, line 65-col. 4, line 6]; the monitoring and generating occurring while operating the hardware element at the first power consumption level [col. 2, lines 29-41]; and in response, throttling the hardware element to operate at a second power consumption level that is a reduced power consumption level than the first power consumption level [col. 1, lines 56-67; col. 2, lines 12-20; col. 3, lines 37-40].

As per claim 2, Bui teaches of monitoring and generating are performed by the power supply [col. 1, lines 62-64].

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[1] Bui is cited in prior office action.

As per claim 3, Bui teaches that the hardware element operates at a first clock frequency when operating at the first power consumption level; and the throttling of the hardware element comprises switching the hardware element to operate at a second clock frequency slower than the first clock frequency [col. 1, lines 56-67; col. 2, lines 12-20; col. 3, lines 37-40].

As per claim 4, Bui teaches that the hardware element operates at a first voltage when operating at the first power consumption level; and the throttling of the hardware element comprises switching the hardware element to operate at a second voltage lower than the first voltage [col. 1, lines 56-67; col. 3, lines 37-40].

As per claim 5, Bui teaches that the hardware element comprises a processor and the throttling of the hardware element comprises periodically interrupting a processor clock [col. 1, lines 56-67; col. 3, lines 37-40].

As per claim 6, Bui teaches that the hardware element comprises a elected one of a processor and a chipset [fig. 2; col. 1, lines 56-67; col. 3, lines 37-48].

As per claim 9, Bui teaches that the hardware element comprises a processor [fig. 2]; and the throttling comprises a chipset in response to the signal, signaling the processor to switch from operating at the first power level of consumption to the second power level of consumption [col. 1, lines 56-67; col. 3, lines 37-40].

4. As per claim 10, Bui teaches a method of operation comprising:

monitoring for re-presence of AC to a power supply of a device after an earlier absence of AC to the power supply [col. 4, lines 26-30]; generating a signal to indicate the presence of AC on detection of re-presence of AC to the power supply; and

throttling a hardware element to operate at a first power consumption level from operating at a second power consumption level in response to the signal, the second power consumption level being a reduced power consumption level than the first power consumption level [col. 1, line 56-col. 2, line 3; col. 2, lines 12-20; col. 3, line 60-col. 4, line 6].

As per claim 11, Bui teaches of monitoring and generating are performed by the power supply [col. 1, lines 62-64].

As per claim 12, Hayashi teaches that the hardware element operates at a first clock frequency when operating at the first power consumption level, and at a second clock frequency when operating at the second power consumption level, the first clock frequency being faster than the second clock frequency; and the throttling of the hardware element comprises switching the hardware element from operating at the second clock frequency back to operating at the first clock frequency [col. 1, lines 56-67; col. 2, lines 12-20; col. 3, lines 37-40].

As per claim 13, Hayashi teaches that the hardware element operates at a first voltage when operating at the first power consumption level, and at a second voltage when operating at the second power consumption level, the first voltage being higher than the second voltage; and the throttling of the hardware element comprises switching the hardware element from operating at the second voltage to operating at the first voltage [col. 1, lines 56-67; col. 2, lines 12-20; col. 3, lines 37-40].

As per claim 14, Hayashi teaches that the hardware element comprises a processor and the throttling of the hardware element comprises ceasing interruption a processor clock [col. 1, lines 56-67; col. 3, lines 37-40].

As per claim 15, Hayashi teaches that the hardware element comprises a Processor [fig. 2]; and the throttling comprises a chipset in response to the signal, signaling the processor to switch to operate at the first power consumption level, from operating at the second power consumption level [col. 1, lines 56-67; col. 2, lines 12-20; col. 3, lines 37-40].

Claim Rejections - 35 USC § 103

5. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui (Bui), U.S. patent no. 6,763,478 as applied to claim1 above, and further in view of Lioux et al. (Lioux), U.S. patent no. 6,274,949.

Bui does not explicitly teach of waiting for a period of time; and initiating a process to suspend the apparatus to memory, if AC remains absent to the power supply after waiting for the period of time.

Lioux teaches of waiting for a period of time [col. 5, lines 64-67]; and initiating a process to suspend the device to memory, if AC remains absent to the power supply after waiting for the period of time [fig. 4; col. 4, lines 55-61; col. 6, lines 5-7].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Bui and Lioux because they both teach a power supply system the specify teachings of Lioux stated above would improve the reliability of Bui system by enter suspend state after absence of AC power.

As per claim 8, Lioux teaches of canceling the wait if AC returns during the waiting period [col. 6, lines 5-7].

Response to Arguments

6. Applicant's arguments filed 2/27/2007, which have been fully considered but they are not persuasive. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

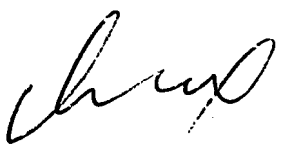
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April. 26, 2007



CHUN CAO
PRIMARY EXAMINER